AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

LISTING OF CLAIMS:

Claims 1 - 15. (Canceled)

16. (Currently Amended) A memory card comprising:

a substrate having a main surface and rear surface, opposed to the main surface;

a plurality of first electrodes formed on the main surface;

a plurality of second electrodes formed on the main surface;

a plurality of external connection terminals on the rear surface;

a first semiconductor chip having a main surface and including a memory circuit and a plurality of bonding pads formed on the main surface thereof, the first semiconductor chip being mounted on the main surface of the substrate;

a second semiconductor chip having a main surface and including a control circuit to control the memory circuit and a plurality of bonding pads formed on the main surface thereof, the second semiconductor chip being stacked over the main surface of the first semiconductor chip;

first wires electrically connecting each of the bonding pads of the first semiconductor chip with a corresponding one of the plurality of first electrodes;

second wires electrically connecting each of the bonding pads of the second semiconductor chip with a corresponding one of the plurality of second electrodes; and

a resin sealing the first semiconductor chip, the second semiconductor chip, the first wires, the second wires and the pluralities of first and second ~~electrodes.~~electrodes,

22. (Previously Presented) A memory card according to claim 21, wherein the second semiconductor chip covers a plan view area that is smaller than that of the first semiconductor chip.

23. (Previously Presented) A memory card according to claim 17, wherein the second semiconductor chip covers a plan view area that is smaller than that of the first semiconductor chip.

24. (Previously Presented) A memory card according to claim 16, wherein the memory circuit is a flash memory.

25. (Previously Presented) A memory card according to claim 16, wherein each of the first semiconductor chip and the second semiconductor chip has a rear surface, opposed to the main surface thereof, that is polished to reduce the thickness of each chip.

26. (Previously Presented) A memory card according to claim 25, wherein the memory circuit is a flash memory.

27. (Previously Presented) A memory card according to claim 16, wherein the second semiconductor chip covers a plan view area that is smaller than that of the first semiconductor chip.

28. (Previously Presented) A memory card according to claim 27, wherein the memory circuit is a flash memory.

29. (Previously Presented) A memory card comprising:

a substrate having a main surface and a rear surface, opposed to the main surface;

a plurality of first electrodes formed on the main surface;

a plurality of second electrodes formed on the main surface;

a plurality of external connection terminals on the rear surface;

a first semiconductor chip having a main surface and including a memory circuit and a plurality of bonding pads formed on the main surface thereof, the first semiconductor chip being mounted on the main surface of the substrate;

a second semiconductor chip having a main surface and including a control circuit to control the memory circuit and a plurality of bonding pads formed on the main surface thereof, the second semiconductor chip being stacked over the main surface of the first semiconductor chip;

first wires electrically connecting each of the bonding pads of the first semiconductor chip with a corresponding one of the plurality of first electrodes;

second wires electrically connecting each of the bonding pads of the second semiconductor chip with a corresponding one of the plurality of second electrodes; and

a resin sealing the first semiconductor chip, the second semiconductor chip, the first wires, the second wires and the pluralities of first and second electrodes,

wherein the first electrodes are positioned along one side of the mounted first semiconductor chip, in a plan view thereof, and

wherein the second electrodes are positioned along another side of the mounted first semiconductor chip, in a plan view thereof.

30. (Previously Presented) A memory card according to claim 29, wherein none of the second wires crosses over any of the first wires, with respect to a plan view of the stacking of the first and second semiconductor chips.

31. (Previously Presented) A memory card according to claim 29, wherein the memory circuit is a flash memory.

32. (Previously Presented) A memory card according to claim 29, wherein each of the first semiconductor chip and the second semiconductor chip has a rear surface, opposed to the main surface thereof, that is polished to reduce the thickness of each chip.

33. (Previously Presented) A memory card according to claim 32, wherein the memory circuit is a flash memory.

34. (Previously Presented) A memory card according to claim 29, wherein the second semiconductor chip covers a plan view area that is smaller than that of the first semiconductor chip.

35. (Previously Presented) A memory card according to claim 34, wherein the memory circuit is a flash memory.

36. (Previously Presented) A memory card according to claim 29, further comprising:

a cap covering the main surface of the substrate.

37. (Previously Presented) A memory card according to claim 16, further comprising:

a cap covering the main surface of the substrate.

38. (Previously Presented) A memory card comprising:

a substrate having a main surface and a rear surface, opposed to the main surface;

a plurality of first electrodes formed on the main surface;

a plurality of second electrodes formed on the main surface;

a plurality of external connection terminals on the rear surface;

a flash memory chip having a main surface and including a flash memory circuit and a plurality of bonding pads formed on the main surface thereof, the flash memory chip being mounted on the main surface of the substrate by an adhesive;

a control chip having a main surface and including a control circuit to control the flash memory circuit and a plurality of bonding pads formed on the main surface thereof, the control chip being stacked over the main surface of the flash memory chip by an adhesive;

first wires electrically connecting each of the bonding pads of the flash memory chip with a corresponding one of the plurality of first electrodes;

second wires electrically connecting each of the bonding pads of the control chip with a corresponding one of the plurality of second electrodes;

a resin sealing the flash memory chip, the control chip, the first wires, the second wires, the plurality of first electrodes and the plurality of second electrodes; and

a cap covering the main surface of the substrate,

wherein the size of the flash memory chip is greater than the size of the control chip,

wherein the first wires are crossing over a first side of the flash memory chip, in a plan view thereof,

wherein the second wires are crossing over a second side of the flash memory chip, different from the side over which the first wires are crossing, in a plan view thereof,

wherein the first electrodes are positioned along the first side of the mounted flash memory chip, and

wherein the second electrodes are positioned along the second side of the mounted flash memory chip.

39. (New) A memory card according to claim 16, wherein the size of the first semiconductor chip is greater than the size of the second semiconductor chip.

40. (New) A memory card according to claim 29, wherein the size of the first semiconductor chip is greater than the size of the second semiconductor chip.

41. (New) A memory card according to claim 29, wherein the second wires are crossing over one side of the first semiconductor chip, in a plan view thereof.